

WHAT IS CLAIMED IS:

1. A method of controlling a flash memory system comprising steps of:

modifying the data of a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

checking for the presence or absence of an error of not properly modifying said data of said group of memory units; and

determining the completion of proper modification of said data of said group of memory units provided that an error is detected and said error can be corrected.

2. A method of controlling a flash memory system comprising steps of:

erasing the data written in a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

reading the data written in said group of memory units having said data erased and checking the completion of proper erasure of said data;

counting the number of errors of not being properly erased provided that said data are not properly erased as a result of said checking step; and

determining the completion of proper erasure of said data of said group of memory units provided that the counted number of errors is within a correctable

~~range.~~

3. A method of controlling a flash memory system comprising steps of:

5 writing^a data in a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

 reading the data written in said group of memory units and checking the completion of proper writing of said data;

10 counting the number of errors of not being properly written provided that said data are not properly written as a result of said checking step; and

 determining the completion of proper writing of said data of said group of memory units provided that
15 the counted number of errors is within a correctable range.

4. A flash memory system comprising:

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 a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

 an error detection/correction unit for reading the data written in said group of memory unit and detecting/correcting errors up to a predetermined
 number;

25 an error judgement section for counting the number of errors detected by said error detection/correction unit and determining the completion of proper data

modification of data provided that the number of errors detected by said error detection/correction unit is not greater than said predetermined number.

5. A flash memory system comprising:

a memory cluster having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering erasure of the data written in said memory cluster;

an error detection/correction unit for detecting erase errors in the data read from said memory cluster and correcting erase errors up to n attributable to memory cells;

an error judgement section for counting the erase errors of each memory sector and determining the completion of proper data erasure provided that the (number of memory cells storing unerased data is not greater than m ($1 \leq m \leq n$) in each and every memory sector.

6. A flash memory system comprising:

a memory cluster having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering erasure of

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11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

the data written in said memory cluster;

an error detection/correction unit for detecting erase errors in the data read from said memory cluster and correcting erase errors up to n symbols ($1 \text{ symbol} = k \text{ bits}$, $k \geq 2$) attributable to the data;

a counter unit for counting the number of symbols showing erase errors and contained in each memory sector;

an error judgement section for determining the completion of proper data modification provided that the number of symbols showing erase errors is not greater than m ($1 \leq m \leq n$) in each and every memory sector.

7. A flash memory system comprising:

a memory cluster comprising a plurality of external flash memory cells;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering writing of the data in said memory sectors;

an error detection/correction unit for detecting errors in the data read from said memory cluster and correcting erase errors up to n attributable to flash memory cells;

an error judgement section for counting the number of memory cells defective in terms of writing and contained in each memory sector and determining the completion of proper data writing provided that the

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number of memory cells defective in terms of writing is not greater than n in each and every memory sector.

8. A flash memory system comprising:

memory sectors having a plurality of flash memory cells;

a flash memory control unit for ordering writing of the data in each of said memory sectors;

an error detection/correction unit for detecting write errors in the data read from said memory cluster and correcting write errors up to n symbols (1 symbol = k bits, $k \geq 2$) attributable to the data;

an error judgement section for counting the number of symbols defective in terms of writing as detected by said detection unit and determining the completion of proper data modification provided that the number of symbols showing errors is not greater than m ($1 \leq m \leq n$) in each and every memory sector.

9. A flash memory system comprising:

a memory cluster comprising a plurality of external flash memory cells;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering writing of the data in said memory sectors;

an error detection/correction unit for detecting write errors in the data read from said memory cluster and correcting write errors up to n bits attributable

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11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

to the data;

an error judgement section for counting the number of bits showing write errors and determining the completion of proper data writing provided that the number of bits showing write errors is not greater than m ($1 \leq m \leq n$) bits in each and every memory sector.

10. A flash memory system comprising:

a memory unit, including a plurality of flash memory cells, for storing data which can be electrically changed;

a control circuit for reading out the data stored in said memory unit and for controlling said memory unit in order to change the data stored in said memory unit;

an error detection and correction unit for detecting whether an error has been occurred in read-out data read out by said control circuit and for correcting errors in the read-out data;

an error judgement section, being implemented independent of said error detection and correction unit, for counting the number of failure data regarded as having not been successfully stored in the memory unit;

wherein said flash system settles that changing of data has been successfully done if the number of failure data is not larger than predetermined number, said predetermined number satisfying the condition that the predetermined number of failure data can be

corrected by said error detection and correction unit.

11. The flash memory system according to claim 10,
wherein said predetermined number is one.

12. The flash memory system according to claim 10,
5 wherein a data length of each data stored in said
memory unit is one bit.

13. The flash memory system according to claim 10,
wherein a data length of each data stored in said
memory unit is larger than one bit.

10 14. A flash memory device comprising:

a memory unit, including a plurality of flash
memory cells, for storing data which can be
electrically changed;

15 a control circuit for reading out the data stored
in said memory unit and for controlling said memory
unit in order to change the data stored in said memory
unit;

20 an error judgement section, being included in said
control circuit, for counting the number of failure
data regarded as having not been successfully stored in
the memory unit;

25 wherein, if the number of failure data is not
larger than predetermined number, said control circuit
outputs status data which means that changing of data
has been successfully done.

15. The flash memory device according to claim 14,
wherein said predetermined number is one.

16. The flash memory device according to claim 14,
wherein a data length of each data stored in said
memory unit is one bit.

5 17. The flash memory device according to claim 14,
wherein a data length of each data stored in said
memory unit is larger than one bit.

18. A flash memory device comprising:

a group of memory units, each having a plurality of
flash memory cells adapted to erasing data therefrom
and writing data therein;

an error judgement section for determining the
completion of proper data modification of data provided
that the number of errors detected by an error
detection/correction unit detecting/correcting errors
15 in the data written in said group of memory units is
not greater than a predetermined number.

19. A flash memory device comprising:

20 a group of memory units, each having a plurality of
flash memory cells adapted to erasing data therefrom
and writing data therein;

an error detection/correction unit for reading the
data written in said group of memory unit and
detecting/correcting errors up to a predetermined
number;

25 an error judgement section for counting the number
of errors detected by said error detection/correction
unit and determining the completion of proper data

modification of data provided that the number of errors detected by said error detection/correction unit is not greater than said predetermined number.

20. A computer-readable recording medium storing a program for realizing in a computer:

a function of ordering modification of data to an external memory device containing a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein; and

a function of checking for the presence or absence of an error of not properly modifying said data of said group of memory units and determining the completion of proper modification of said data of said group of memory units provided that an error is detected and said error can be corrected.

21. A computer-readable recording medium storing a program for realizing in a computer;

a function of ordering erasure of the data written in a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein; and

a function of reading the data written in said group of memory units having said data erased and checking the completion of proper erasure of said data, counting the number of errors of not being properly erased provided that said data are not properly erased

as a result of said checking step and determining the completion of proper erasure of said data of said group of memory units provided that the counted number of errors is within a correctable range.

5 22. A computer-readable recording medium storing a program for realizing in a computer;

10 a function of ordering writing of data written in a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein; and

15 a function of reading the data written in said group of memory units and checking the completion of proper writing of said data counting the number of errors of not being properly written provided that said data are not properly written as a result of said checking step and determining the completion of proper writing of said data of said group of memory units provided that the counted number of errors is within a correctable range.

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